Analysis of impedance and current distributions in parallel IGBT design

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***Abstract*—Power electronic applications need high voltage and current ranges which are impossible to obtain with discrete devices. Parallelization technique is a solution to increase power converter current capacity. Current distribution problems may reduce device lifetime and cause converter malfunction. Parallelization requires a total control of circuit parasitic elements which depend on layout physical materials and dimensions. The objective of this article is to show, by electromagnetic (EM) model simulations, layout non ideal effects for power circuits, in order to understand and control circuit stray elements, especially parasitic inductances, and current distributions.**

***Index Terms*—Parallelization, layout, parasitic inductance (L_p), current distribution, coupling parasitic effect (M_p), simulation, EM model, non ideal effects, ADS^{TM}.**

I. Introduction

Nowadays, power electronic applications need higher voltage and current ranges. These ranges are out of operational limits of discrete chips and power modules, and they are only possible with serial and parallel configurations. A solution to improve power converter density is to use the parallelization of discrete devices, because of increasing current capacity. Parallel designs are composed of several dies in parallel where current imbalances appear due to physical properties of the design. For parallel proper operation, power semiconductor current distributions should be as equal as possible, since imbalances reduce the device lifetime and deteriores electrical properties of the design [1], [2]. The design depends on semiconductor characteristic parameters ($V_{ce_{sat}}$, delays $t_{d_{on}}$ and $t_{d_{off}}$, temperature coefficient, etc), gate-emitter (Z_{ge}) and collector-emitter (Z_{ce}) impedances [3], [4].

Power printed circuit board (PCB) or direct bonded copper (DBC) presents structural parasitic impedances such as path inductances and resistances with their substrate capacitances (figure 1) [5]. It is important to analyse the parasitic inductance effets because their di_L/dt generates voltage drops and current peaks which affect circuit operation [6], [7]. In a power module design, controlling layout physical dimensions are fundamental to use each chip at maximum ratings. For this reason, layout needs to be as symmetrical as possible disposing power semicondutctors, linking traces and external pins, so overvoltages and current imbalances are reduced [8]. Moreover, power modules operate at higher frequencies and designs are more compact, so the effects of parasitic inductance coupling increases electromagnetics emissions [9]. Besides, the equivalent mesh models are more complex. It is essential to develop EM model simulations to understand current distributions and to predict circuit behaviour [10], [11].

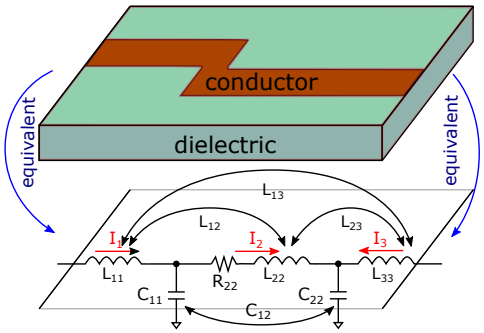


Fig. 1. Parasitic elements of paths in power layouts.

The present work analyses layout impedances, voltages and current distributions of four different switch designs with four parallel IGBT. The aim is to compare simulations, using Keysight ADS^{TM} software, of these basic power layout designs to understand the variations due to different geometries during switching state. The study helps in establishing criteria in order to develop a good power converter design.

II. Electrical equivalent circuit

The power converter design requires an analytical model to take into account layout non ideal effects for designs with hundreds of paths and connections.

A. Extraction of layout parasitic elements

The parasitic elements in a power circuit can be represented by partial element equivalent circuit (PEEC) where each layout structure can be modelled by resistance (R), autoinductance (L_p) and mutual coupling inductance (M_p) between traces [1], [7], [12], [13]. Figure 2 shows the PEEC equivalent circuit of two rectangular loops with one segment in common. The electrical loop behaviour depends on circuit elements proportional to coplanar physical l, w and t dimensions (figure 3) and some material characterisitics as resistivity, ρ, and permeability, μ. Then, each path or trace is simplified as R (1), L_p (2) and M_p (3) for low frequencies (<1 MHz) [14]–[16]. Moreover, M_p depends on current direction to be added or subtracted in the total loop inductance value (L_{loop}). In the circuit shown in figure 2, M_p values are added because loops have the same current direction through inductances, so L_{loop_1} and L_{loop_2} can be obtained as (4) and (5), and total mutual inductance M_{12} is (6).

$$R = \rho \cdot l \cdot 10^3 \cdot w/t; \tag{1}$$

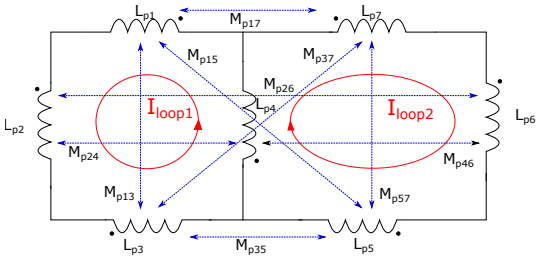


Fig. 2. Two loops with one common segment solving with PEEC.

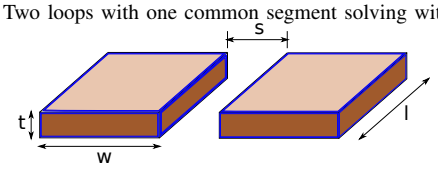


Fig. 3. Coplanar plate inductance geometrical dimensions.

$$L_{pi} = 0.00508 \cdot \left(\frac{l}{25.4}\right) \cdot \cdot \left(2.303 \cdot log_{10}\left(\frac{2 \cdot l}{w+t}\right) + 0.5 + 0.2235 \cdot \frac{w+t}{l}\right); \quad (2)$$

$$M_{pij} = \frac{\mu}{\pi} \cdot cosh^{-1}\left(\frac{w+s}{w}\right) \cdot l. \quad (3)$$

$$L_{loop1} = L_{p1} + L_{p2} + L_{p3} + L_{p4} + 2M_{p24} + 2M_{p13}; \quad where\ M_{p24} = M_{p42};\ M_{p13} = M_{p31}; \quad (4)$$

$$L_{loop2} = L_{p4} + L_{p5} + L_{p6} + L_{p7} + 2M_{p46} + 2M_{p57}; \quad where\ M_{p46} = M_{p64};\ M_{p57} = M_{p75}; \quad (5)$$

$$M_{12} = M_{21} = M_{p15} + M_{p17} + M_{p24} + M_{p26} + M_{p37} + M_{p35} + M_{p46} + L_{p4}. \quad (6)$$

However, in the layout design there are several number of interconnections with their coupling inductances. The electrical model becomes very complex to be solved analitically and only provides a constant current density [17]. For this reason, other methods are necessary to calculate stray elements effects.

B. Mesh model development for non ideal circuit simulations

The PEEC analytival method were developed some years ago [7], [12], [13]. An electrical simulator is necessary to process thousands of connections. Besides, with a 3D mesh is possible to show non uniformities in current distribution taking into account two perpendicular directions [2], [17]. Keysight ADS^{TM} software provides a tool to analyse the design equivalent impedances. The software is based on input/output microwave technology to get the scattering matrix (7) [18] for a particular frequency.

$$S_{ij} = \left.\frac{V_i^-}{V_j^+}\right|_{V_k^+=0\ for\ k\neq j} \quad (7)$$

For each design, S-parameters are calculated for 0 Hz - 1 MHz (low frequency) with 2.5 kHz step. The mesh is formed by a lot of cells which include parasitic elements (figure 1). Then, a co-simulation between power semiconductor electrical models and the layout S-parameters give a non ideal circuit behaviour during transit simulation which helps to understand voltage and current distributions.

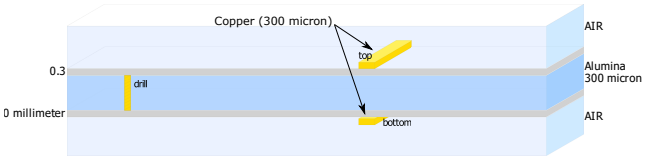


Fig. 4. Substrate used in the designs.

III. Parallelization Design Technique

In order to develop a correct design for power converters with devices in parallel it is fundamental to control transistor currents, since parasitic inductances produce drop voltages and high current peaks.

The aim of this section is to simulate different layouts of the same basic circuit to study parallelization effects, especially current density distribution, due to the differences in physical geometries and stray impedances. The switch circuit consists of 4 parallel IGBTs (IGBT AUIR4067D1, 600 V/160 A) in different topologies connected to a load. The configurations for this switch circuit are shown in the figure 5:

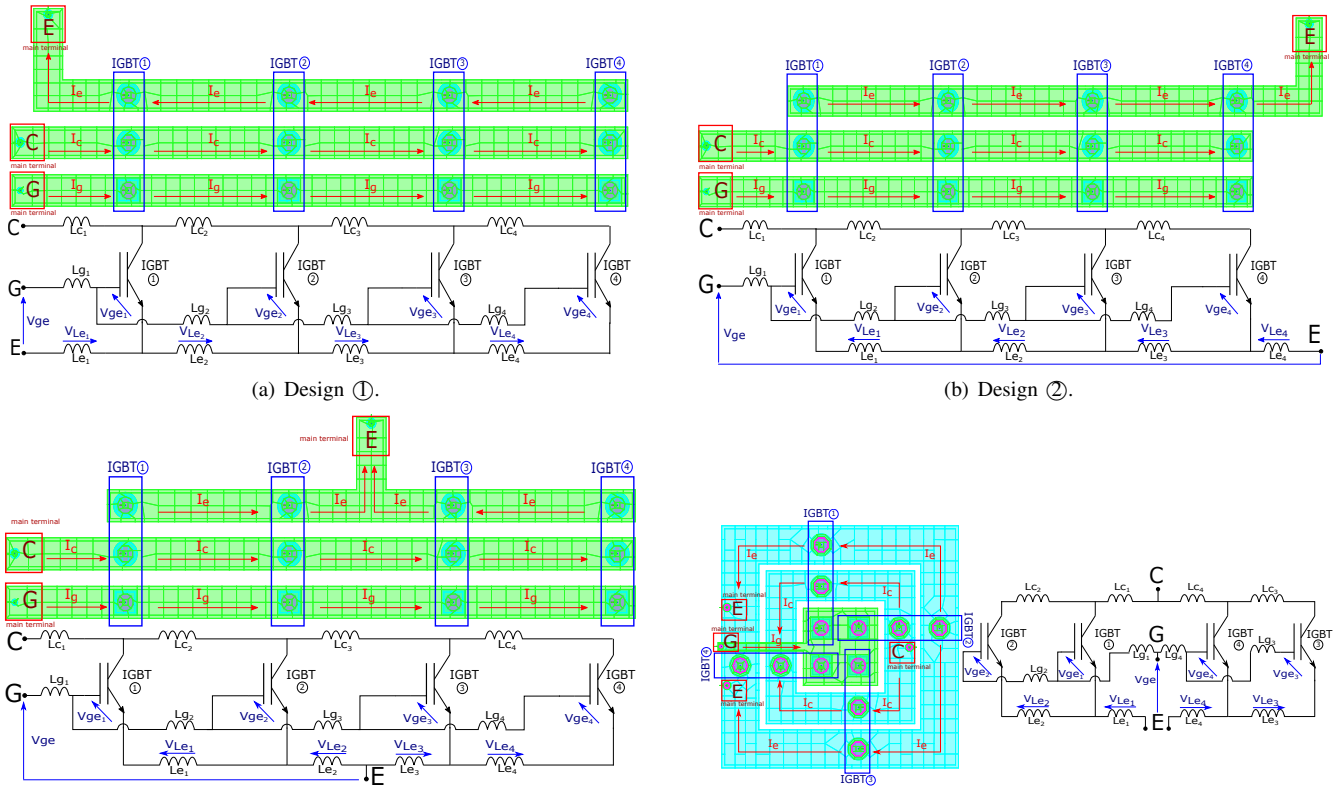
1) Design ① (figure 5(a)) is a linear topology connection of IGBTs. The main terminals (gate, collector and emitter) are in the same side of layout, I_c and I_e path currents have opposite directions.
2) Design ② (figure 5(b)) is similar to design ①, but the emitter main terminal is in the opposite side, so I_g, I_c and I_e path currents have the same direction.
3) In design ③ (figure 5(c)) the emitter main terminal appears in the middle of the trace. For this, there are two I_e current directions in the same path, like a mix between design ① and ②.
4) Design ④ (figure 5(d)) presents IGBTs in a square configuration around their gates (symmetric concept) and in two layers (top and bottom) with a better coupling effect (parallel plate) [15].

Once layout design is defined, the first step is to obtain the equivalent impedances (Z_{ge} and Z_{ce}) between input/output common terminals with each IGBT terminals. The equivalent path resistances and inductances are calculated, the gate voltage signals (gate-emitter close loop) and IGBT currents (collector-emitter close loop) are analysed to understand parallelization in each proposed design.

A. Extraction of Z_{ge} and Z_{ce} equivalent impedances

In order to calculate Z_{ge} and Z_{ce} impedances gate-emitter and collector-emitter close loops, the substrate topology has to be analysed (figure 4), because impedances depend on material properties.

The gate-emitter close loop gives the equivalent Z_{ge} impedances value between gate and emitter main terminals with each IGBT gate and emitter. Measurements in collector-emitter close loop also give the equivalent Z_{ce} values between collector and emitter main terminals with each IGBT collector



(a) Design ①. (b) Design ②.

(c) Design ③. (d) Design ④.

Fig. 5. Layout designs of a parallel switch with their equivalent circuit.

and emitter. The impedance values are extracted from S-parameters matrix in complex numbers and a conversion is applied to obtain R and L values. It is necessary to transform S-parameters in Y-parameters (8), since Y_{11} parameter gives directly the equivalent admittance value short-circuiting the load [18]. The R and L values are calculated applying (9).

$$Y_{ij} = \left.\frac{I_i}{V_j}\right|_{V_k=0 \ for \ k\neq j} ; \tag{8}$$

$$R = Real\left(\frac{1}{Y_{11}}\right) ; \ L = \frac{Imag\left(\frac{1}{Y_{11}}\right)}{2 \cdot \pi \cdot freq}. \tag{9}$$

Tables I(a) and I(b) show R and L gate-emitter close loop (R_{ge} and L_{ge}) and collector-emitter close loop (R_{ce} and L_{ce}) for 10 kHz (modulation frequency of the power converter). The results show that design ④ has the lowest R_{ge}, L_{ge}, R_{ce} and L_{ce} values, due to its symmetrical topology, short paths and better coupling effect.

However, design ② presents maximum Z_{ge} and Z_{ce} values, so losses in these traces are high. But variations between R_{ge}, L_{ge}, R_{ce} and L_{ce} are minimum, so that the current per each IGBT is more evenly distributed, producing lower imbalances than in other designs. This is because I_g, I_c and I_e currents have the same direction in layout traces.

The main different between design ① and ② is the I_e current direction, and for this, impedance values are different because of mutual coupling effects. The values R_{ge}, L_{ge}, R_{ce}

TABLE I
Z_{ge} AND Z_{ce} MEASURES FOR EACH DESIGN AT 10 KHZ.
(a) Z_{ge} gate-emitter impedance.

Design	Gate - Emitter Loop											
	IGBT1		IGBT2		IGBT3		IGBT4		Max. Variation		Maximum	
	Rge (mΩ)	Lge (nH)	Rge (mΩ)	Lge (nH)	Rge (mΩ)	Lge (nH)	Rge (mΩ)	Lge (nH)	Rge (mΩ)	Lge (nH)	Rge (mΩ)	Lge (nH)
1	0.67	12.68	1.34	31.47	2.00	50.65	2.67	69.90	1.99	57.22	2.67	69.90
2	1.64	72.01	1.64	72.32	1.64	72.32	1.65	72.58	0.01	0.56	1.65	72.58
3	0.99	33.46	1.00	33.53	1.33	43.15	1.99	62.14	1.00	28.69	1.99	62.14
4	0.90	11.93	1.03	16.59	0.97	14.48	0.73	8.70	0.30	7.89	1.03	16.59

(b) Z_{ce} collector-emitter impedance.

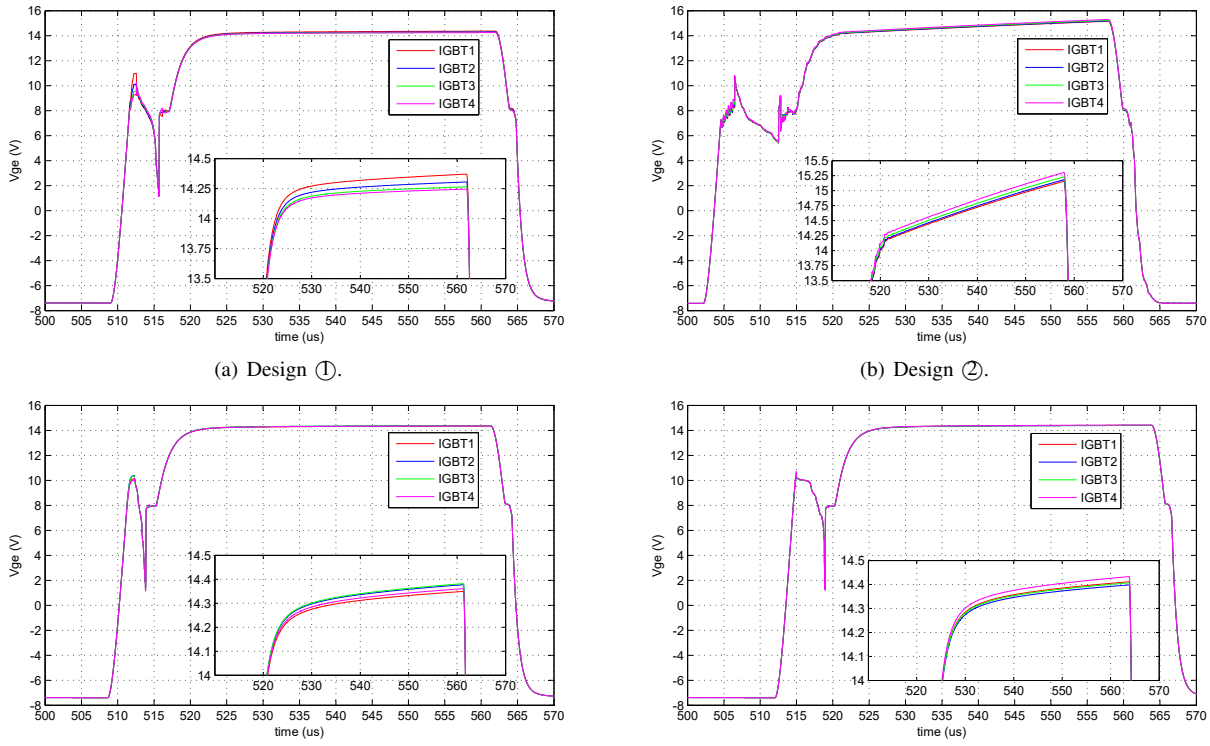
Design	Collector - Emitter Loop											
	IGBT1		IGBT2		IGBT3		IGBT4		Max. Variation		Maximum	
	Rce (mΩ)	Lce (nH)	Rce (mΩ)	Lce (nH)	Rce (mΩ)	Lce (nH)	Rce (mΩ)	Lce (nH)	Rce (mΩ)	Lce (nH)	Rce (mΩ)	Lce (nH)
1	0.64	10.86	1.29	24.28	1.94	37.80	2.59	51.33	1.96	40.47	2.59	51.33
2	1.61	73.17	1.62	73.09	1.62	73.04	1.63	73.04	0.02	0.14	1.63	73.17
3	0.96	34.10	0.97	34.07	1.30	40.85	1.95	54.32	0.99	20.25	1.95	54.32
4	0.50	12.38	0.45	13.70	0.50	12.18	0.39	8.01	0.11	5.68	0.50	13.70

and L_{ce} of ① are lower than design ②, but variations between IGBT branches are higher.

Design ③, with the emitter in the middle, reduces R_{ge}, L_{ge}, R_{ce} and L_{ce} values compared with design ①, but it is not enough compared with designs ② and ④.

B. Gate-emitter close loop influence on V_{ge} signals

Connection between IGBTs and driver circuit (gate connection) generate a close gate-emitter loop where different feedback effects produce variations between parallel IGBTs



(a) Design ①.

(b) Design ②.

(c) Design ③.

(d) Design ④.

Fig. 6. V_{ge} voltage signals for different designs of a 4 parallel IGBTs switch.

gate voltage signals (V_{ge}). These V_{ge} signal variations affect the turn off process, generating differences in switching losses.

Different feedback effects are produced in the designs because of emitter topology and equivalent inductances (tables I(a) and I(b)). The following equations only take into account the emitter inductances (the most critical because $\frac{di_e}{dt} >> \frac{di_g}{dt}$) to simplify the behaviour of feedback effects ($L_{e_i} \neq L_{ge_i}$):

1) Design ① presents a negative asymmetric feedback (figures 5(a) and 6(a)) causing IGBT4 to turn on slower than IGBT1 because of the inductances ($L = L_{e_2} = L_{e_3} = L_{e_4} \neq L_{e_1}$) which generate voltage drops ($V_L = V_{L_{e_2}} = V_{L_{e_3}} = V_{L_{e_4}} \neq V_{L_{e_1}}$) (10).

$$\begin{aligned} &V_{ge_4} = (V_{ge} - 3 \cdot V_L - V_{L_{e_1}}) < V_{ge_3} = \\ &= (V_{ge} - 2 \cdot V_L - V_{L_{e_1}}) < V_{ge_2} = \\ &= (V_{ge} - V_L - V_{L_{e_1}}) < V_{ge_1} = (V_{ge} - V_{L_{e_1}}). \end{aligned} \tag{10}$$

2) Design ② has a positive asymmetric feedback (figures 5(b) and 6(b)), so IGBT1 is turned on faster than IGBT4, in (11) taking into account inductances ($L = L_{e_1} = L_{e_2} = L_{e_3} \neq L_{e_4}$) and voltage drops ($V_L = V_{L_{e_1}} = V_{L_{e_2}} = V_{L_{e_3}} \neq V_{L_{e_4}}$) simplifications.

$$\begin{aligned} &V_{ge_1} = (V_{ge} - 3 \cdot V_L - V_{L_{e_4}}) < V_{ge_2} = \\ &= (V_{ge} - 2 \cdot V_L - V_{L_{e_4}}) < V_{ge_3} = \\ &= (V_{ge} - V_L - V_{L_{e_4}}) < V_{ge_4} = (V_{ge} - V_{L_{e_4}}). \end{aligned} \tag{11}$$

3) Design ③ is a positive and negative feedback (figures 5(c) and 6(c)), because there are emitter currents in two directions. Mutual inductances have an important effect causing that $L_{e_3} < L_{e_2} < L_{e_4} < L_{e_1}$ and voltage inductance drops $V_{L_{e_3}} < V_{L_{e_2}} < V_{L_{e_4}} < V_{L_{e_1}}$(12).

$$\begin{aligned} &V_{ge_3} = (V_{ge} - V_{L_{e_3}}) > V_{ge_2} = (V_{ge} - V_{L_{e_2}}) > \\ &> V_{ge_4} = (V_{ge} - V_{L_{e_3}} - V_{L_{e_4}}) > V_{ge_1} = \\ &= V_{ge} - V_{Le_1} - V_{Le_2}. \end{aligned} \tag{12}$$

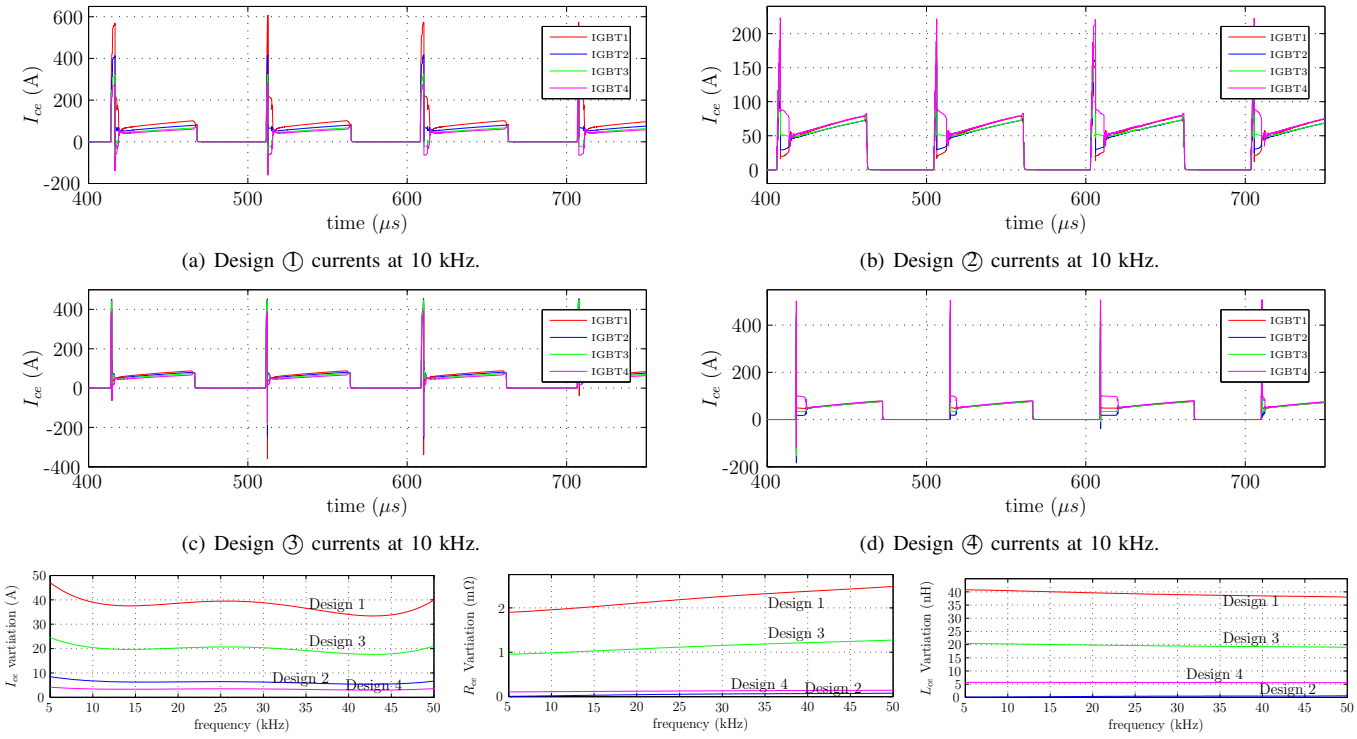
4) Design ④ works like two positive asymmetric feedback (figures 5(d) and 6(d)) because of trace lengths $L_{e_4} < L_{e_1}$ and $L_{e_3} < L_{e_2}$, so voltage emitter inductance drops are $V_{L_{e_4}} < V_{L_{e_1}}$ and $V_{L_{e_3}} < V_{L_{e_2}}$ (13).

$$\begin{aligned} &V_{ge_4} = (V_{ge} - V_{Le_4}) > V_{ge_1} = (V_{ge} - V_{Le_1}) > \\ &V_{ge_3} = (V_{ge} - V_{Le_4} - V_{Le_3}) > V_{ge_2} = \\ &= (V_{ge} - V_{Le_1} - V_{Le_2}). \end{aligned} \tag{13}$$

Designs ② and ④, which present lower Z_{ge} and Z_{ce} variations, have lower V_{ge} voltage drops between IGBTs because of this voltage behaviour. The currents through IGBTs are more balanced. However, design ① presents a wide V_{ge} variation because its emitter inductances are very unequal, causing high imbalances between IGBT currents. Design ③ has two different V_{ge} (two I_e current directions in the same copper trace) levels proportional to the distance between each IGBT emitter and main emitter layout terminal.

C. Collector-emitter close loop influence on I_{ce}

Parallel IGBTs have different current distribution because of trace connections. Apart from IGBT gate and driver connections, which generate delays between device gate signals



(a) Design ① currents at 10 kHz.

(b) Design ② currents at 10 kHz.

(c) Design ③ currents at 10 kHz.

(d) Design ④ currents at 10 kHz.

(e) I_{ce} variation 5-50 kHz.

(f) R_{ce} variation 5-50 kHz.

(g) L_{ce} variation 5-50 kHz.

Fig. 7. IGBT currents for the designs and I_{ce}, R_{ce} and L_{ce} variations with frequency.

(V_{ge}), the path between collectors and emitter of the IGBTs is a critical parameter. The designs have different current distribution which is analysed in the figure 7:

1) Design ① presents the worst current distribution for 10 kHz switching signals (figure 7(a)) with 47 A current variation due to the high differences between Z_{ce} IGBT values and its linear topology.
2) Design ② has similar current per IGBT branch (figure 7(b)) with only maximum variation of 8.5 A. Moreover, turn on initial oscillation is lower than in other design due to higher Z_{ce} values compared with the other designs impedances. In spite of its linear geometry, coupling effects compensate its dimensions, due to current directions.
3) Design ③ has the same problems as ①. The current distribution presents a maximum 24.5 A variation between IGBTs at 10 kHz (figure 7(c)) because R_{ce} and L_{ge} are very different between parallel IGBTs. However, results are better, since emitter main terminal gives to design more symmetry.
4) Design ④ has the best current distribution between IGBT branches with a maximum variation of 4.1 A at 10 kHz (figure 7(d)), due to symmetrical dimensions and equal values of Z_{ce} between IGBTs and main terminals.

IGBT current distribution depends on R_{ce} and L_{ce}. When these values are very unequal between IGBTs and layout main terminals, current distribution presents wide variations, like in designs ① and ③. However, if R_{ce} and L_{ce} values are similar, current variations are lower, like designs ② and ④. This kind of behaviour is shown in figures 7(e), 7(f) and 7(g) and it is stable between 5 - 50 kHz (switching frequency range to silicon power modules).

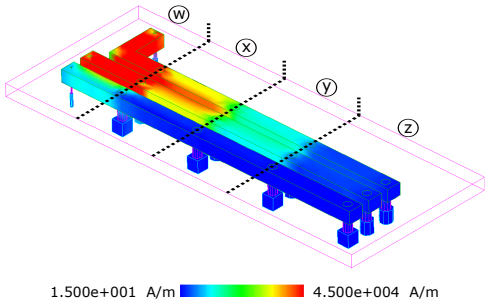
D. Current density distributions

Current distribution depends on Z_{ge} and Z_{ce}, proportional to physical dimensions, V_{ge} voltage signals, which generate delays between parallel IGBTs, and current direction, because of adding/substrating mutual coupling effects.

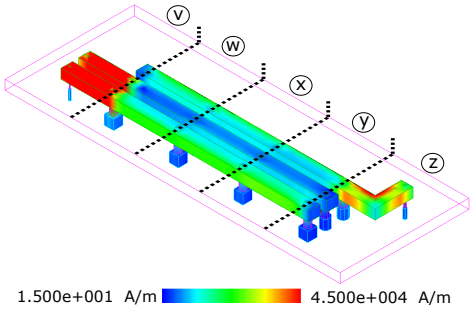
According to V_{ge} signals and I_{ce} IGBT currents, design ① (figure 8(a)) and ② (figure 8(b)) present bad current density distribution on layout, because in both designs 10 kHz signals present the ⓦ area with a high current density, when the rest of paths have lower density, because design ① and ② are not symmetrical. Design ③ presents a better current density distribution (figure 8(c)), since emitter main terminal (ⓨ area) gives to the circuit a symmetrical behaviour at 10 kHz and an equal current emitter distribution, but design ③ presents a higher current density in the ⓦ area which unbalances collector current. Design ④ (figure 8(d)) has the best symmetrical current density distribution, because 10 kHz signals have similar current density through paths of ⓦ and ⓩ areas with high current density levels.

IV. Conclusions

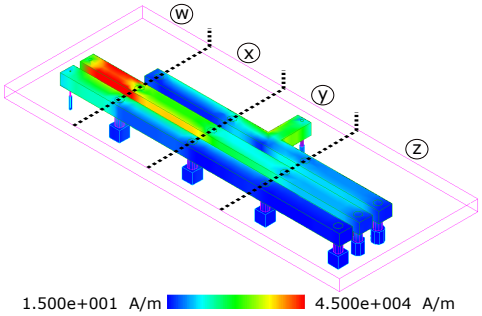
The main problem of parallel design is current distributions which generates current imbalances. These imbalances reduce lifetime of power semiconductor and affect efficiency, so they have to be reduced. Physical geometries and dimensions



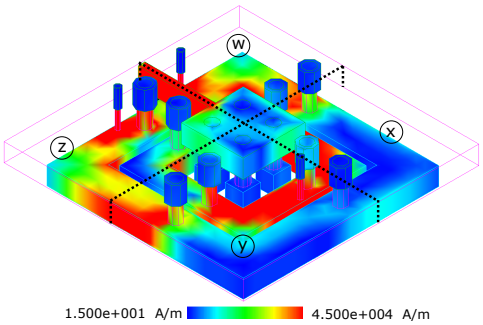
(a) Design ①.



(b) Design ②.



(c) Design ③.



(d) Design ④.

Fig. 8. Current density distribution in 3D layouts at 10 kHz.

of the layout must be properly designed because equivalent circuit impedances depend on path physical forms and materials. Taking into account current directions, since Z_{ge} and Z_{ce} impedance values can increase or decrease with mutual coupling effects. Apart from Z_{ge} impedance values, emitter current direction affects V_{ge} voltage signals of parallel IGBTs, because different feedback effects produce different V_{ge} voltage drops. These V_{ge} signals turn on/off IGBTs with different delays, increasing current imbalances. Finally, for a correct design, Z_{ce} values must be reduced to decrease stray elements losses. However, it is more important that there are minor Z_{ce} variations between parallel connections to have better current distributions than reducing their values.

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